

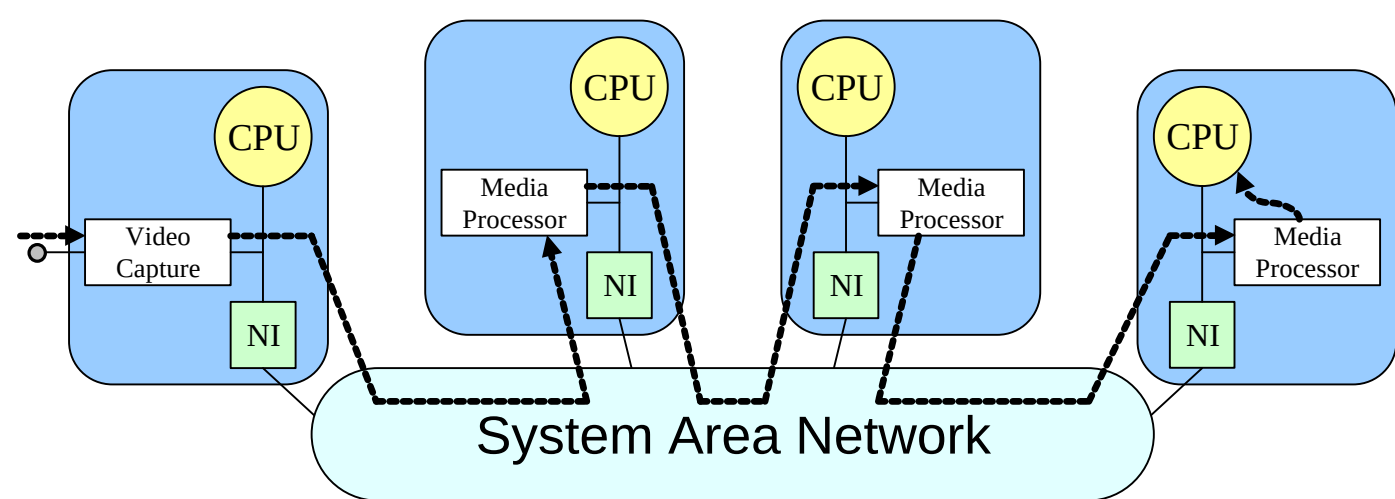
Active System Area Networks (ASAN)

Dr. Ken Mackenzie, Dr. David Schimmel, Dr. Sudhakar Yalamanchili

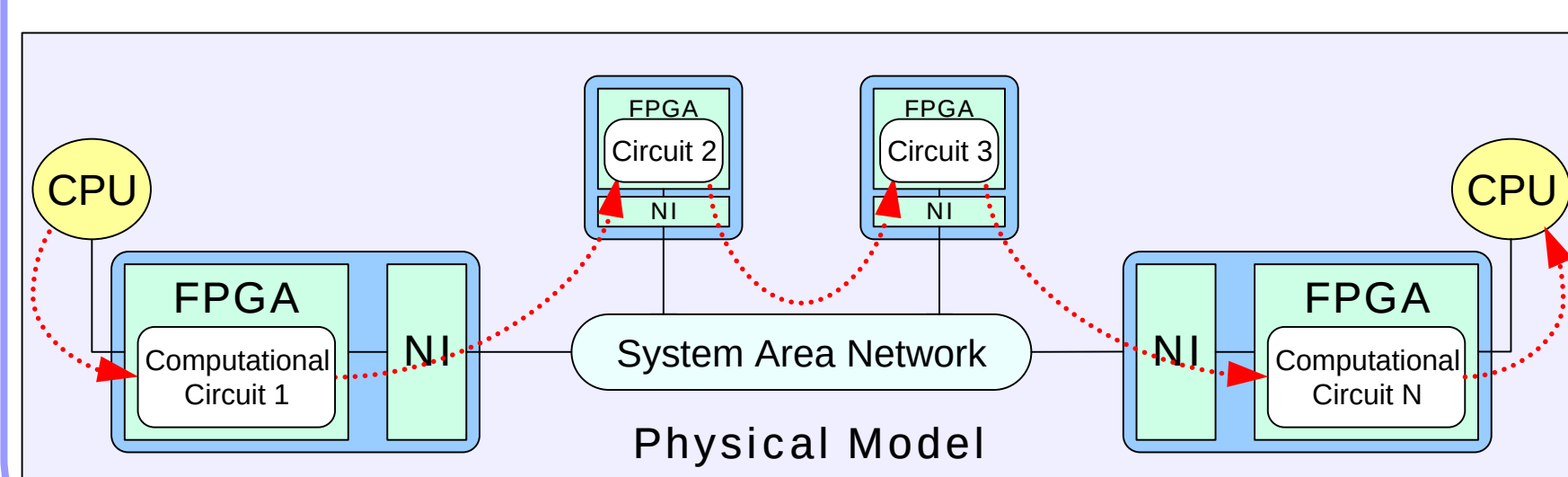
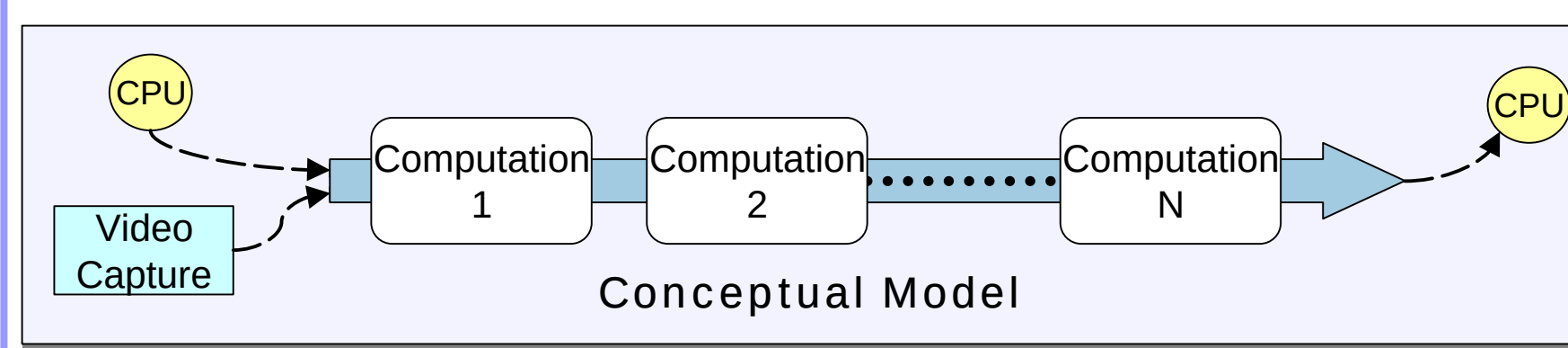
Chris Clark, Adam Johnson, Craig Ulmer, Chris Wood

Concept

- Perform computations on messages *in-transit*
 - FPGAs process data at link speeds
 - Advantage: Usable by CPUs and peripheral devices
 - Examples: Data transformations, Cryptography, Filtering

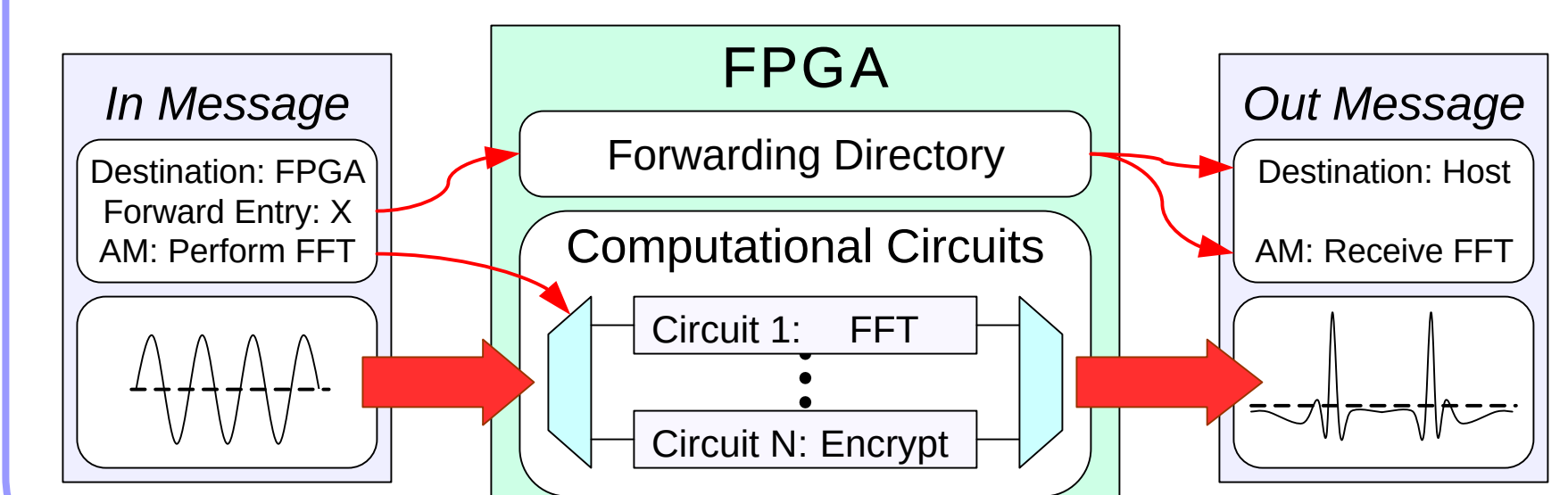


Streaming Computations



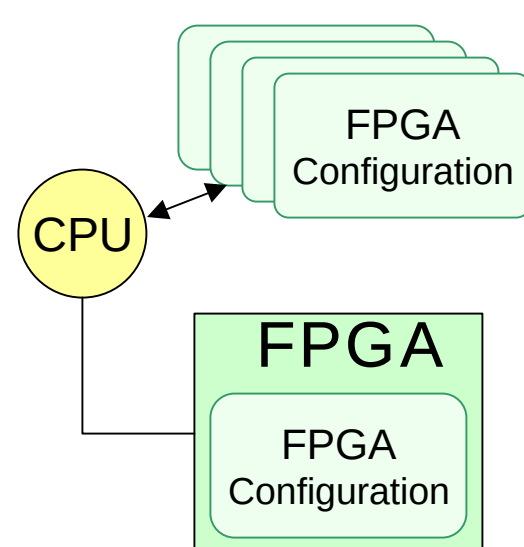
Streaming Details

- Computation:** Which computation performed?
 - Active message approach
- Forwarding:** Where are results sent?
 - Programmable forwarding directory

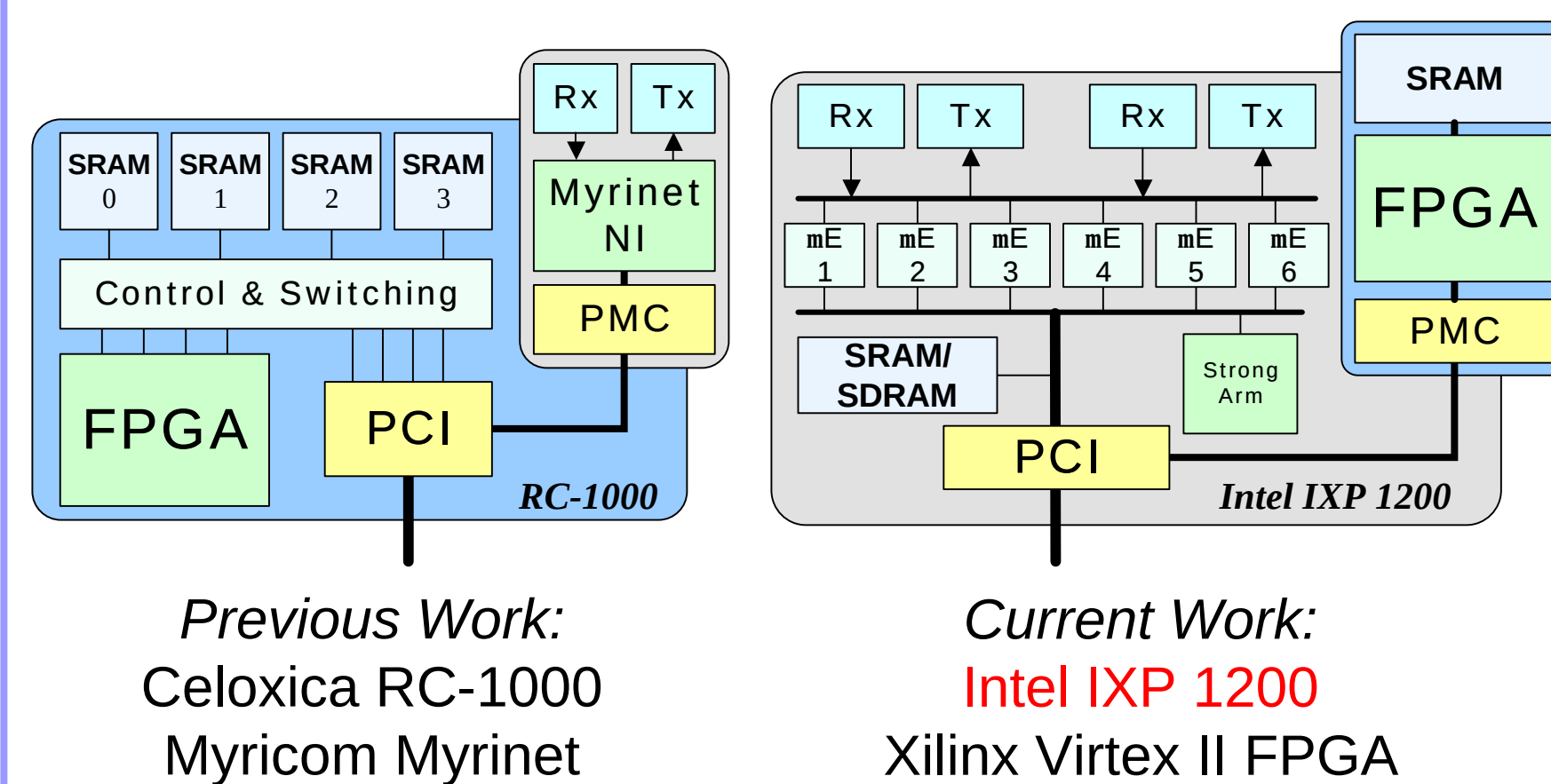


FPGA Reconfiguration

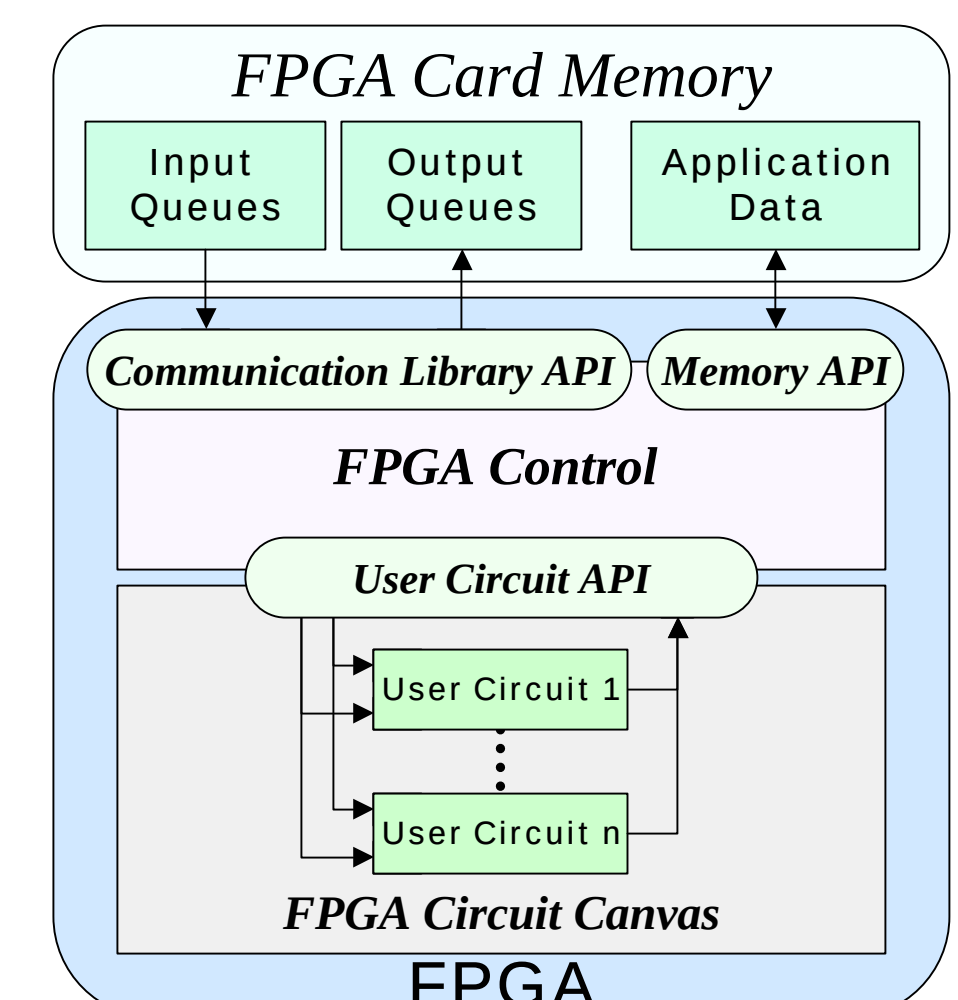
- Demand driven dynamic reconfiguration**
 - Host manages FPGA configurations
- Requested circuit not loaded?**
 - FPGA stores state, generates *function fault*
 - Host loads new configuration
 - FPGA loads state, restarts
- Currently: Full FPGA reconfiguration**
 - Research: Partial run-time reconfiguration



NI-FPGA Prototypes

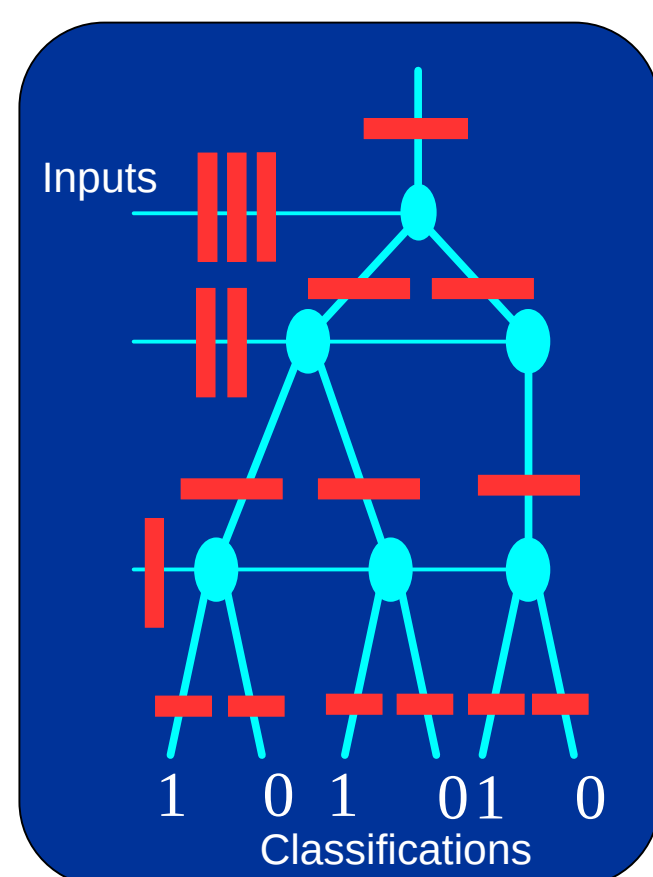


FPGA Interfaces



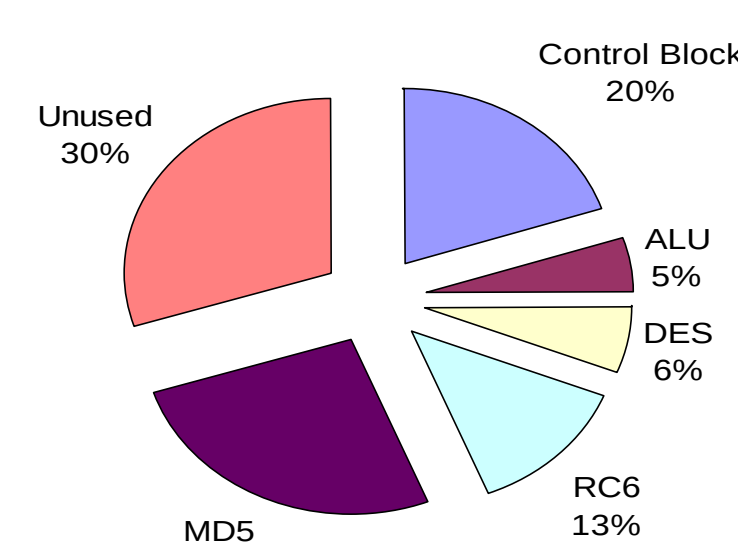
FPGA Example: Pattern Matching for Packet Classification

- Classify IP packets**
 - Pattern matching task
 - Implement in FPGA
- Binary Decision Diagram**
 - Outputs are classification
 - Map BDD to FPGA gates
 - Muxes and registers



FPGA Example: Cryptography

- Cryptography unit**
 - DES, RC6, MD5, ALU
 - Keys set dynamically
 - 73 MB/s for 4KB data
- Full reconfiguration approach**
 - Configure time: 90 ms
 - Possible to create optimized *key-specific configurations*



Conclusions and Future Work

- FPGAs valuable for network processing**
 - Perform custom computations in hardware
 - Adaptable to different problems
- ASAN allows computations to take place in network**
 - Processing in NI and peripheral devices
 - Powered by **GRIM** communication library
- Future work**
 - Partial FPGA reconfiguration mechanisms
 - Selectable computation target (Host, NI, or FPGA)
 - Transition to IXP based Gigabit Ethernet

