

#### A Configurable-Hardware Document-Similarity Classifier to Detect Web Attacks

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# **Overview**

- Network security is challenging, especially at link speed
  - FPGAs offer convenient means of brute-force pattern matching
  - Attackers game network intrusion detection systems
- Network researchers: machine learning for better classification
  - Document Similarity via TFIDF and Cosine Similarity
  - Found >94% accuracy in HTTP attack classification
  - But, slow and utilized 46MB of dictionary data
- Adapt document similarity to an embedded form
  - Simplifications, dictionary reductions, parallel Bloom filters
  - Tools to automatically generate FPGA hardware
  - Achieve 94% accuracy with 128KB dictionary at GigE rates







# Outline

- Introduction
  - Discovery challenge and LLNL approach
- Adapting to embedded hardware
  - Algorithm modifications
  - Data modifications
- Implementation details
  - Core design
  - Tool flow
  - Performance and resource utilization
- Future work

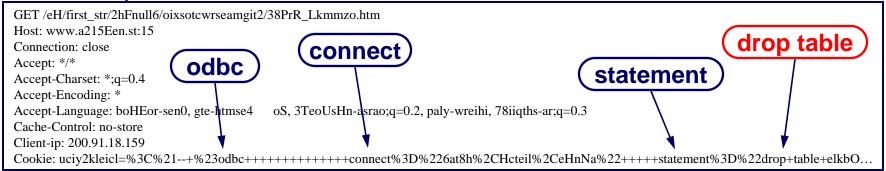




# ECML/PKDD 2007 Discovery Challenge

- HTTP Traffic Classification
  - Apply machine learning to identify malicious activity in HTTP
- Hand-labeled datasets of HTTP flows
  - Training: 50K inputs, 30% attacks
  - Testing: 70K inputs, 40% attacks
  - 7 Attack Types
    - XSS, SQL/LDAP/XPATH injection, path traversal, command execution, and SSI

#### **Flow Example**



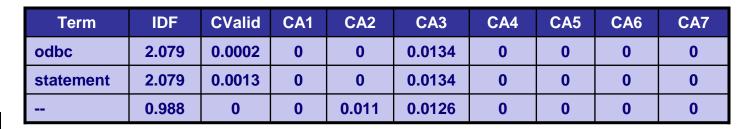


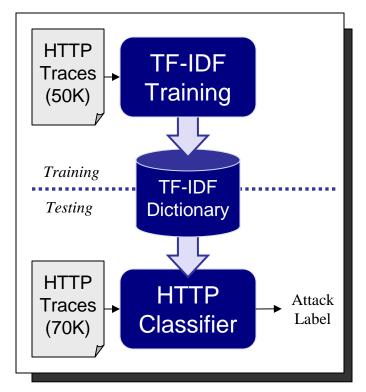




# **Prior LLNL Work**

- Brian Gallagher and Tina Eliassi-Rad
- Document similarity: vector approach
  - Tokenize input
  - Assign weights to tokens via TFIDF
  - Cosine similarity for vector comparison
- Relies on a data dictionary
  - Generate term statistics during training
  - Reference statistics at runtime
  - Each term: IDF value and C weights



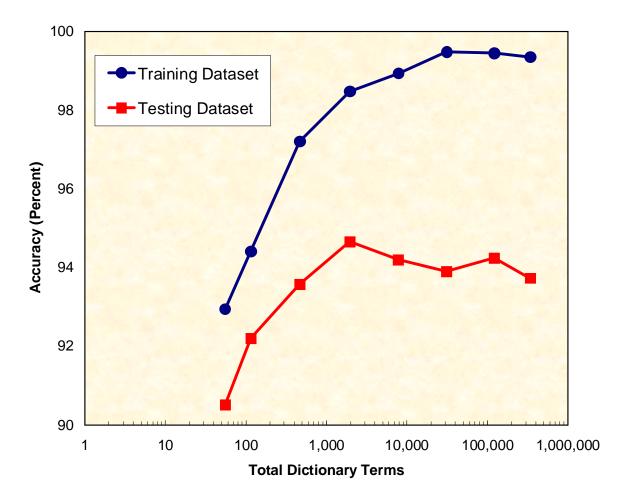








## **Original Accuracy**









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# **Hardware Adaptation Challenges**

- Computation
  - Blocking form
  - Floating point math
  - Divide and square root operations
- Dictionary: 46MB, 1.8M terms
  - Large storage
  - Lookup overhead
- Path for converting to hardware
  - Build the hardware design once
  - Automatically update with configuration data



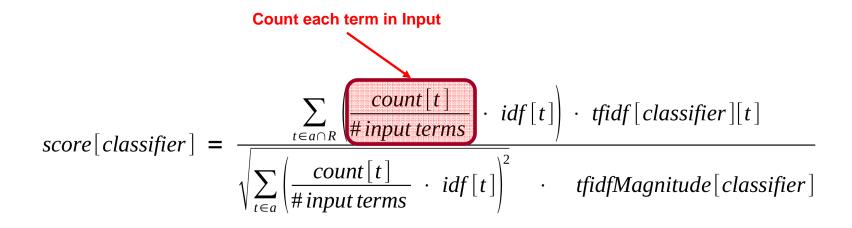




$$score[classifier] = \frac{\sum_{t \in a \cap R} \left( \frac{count[t]}{\#input terms} \cdot idf[t] \right) \cdot tfidf[classifier][t]}{\sqrt{\sum_{t \in a} \left( \frac{count[t]}{\#input terms} \cdot idf[t] \right)^{2}}} \cdot tfidfMagnitude[classifier]$$

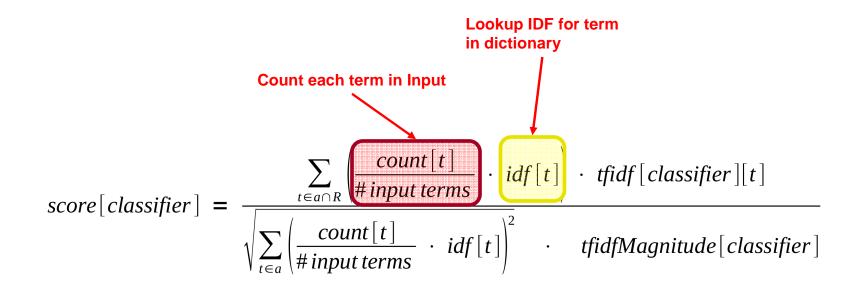






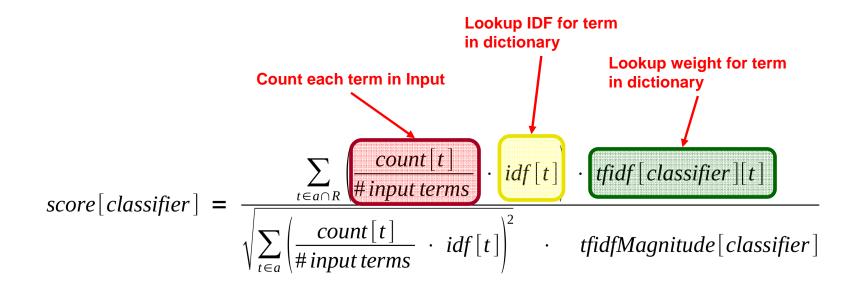






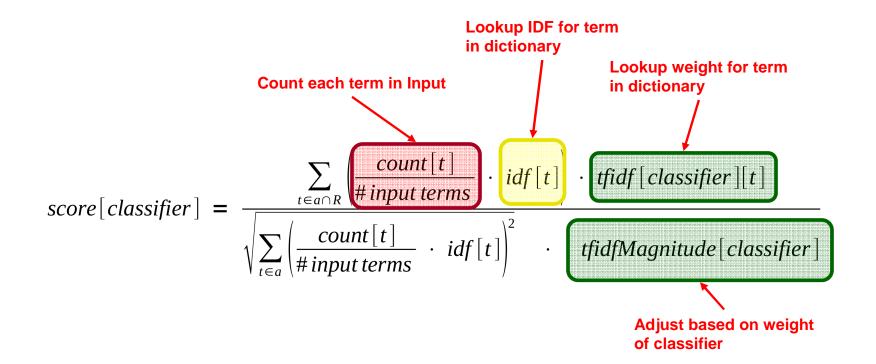






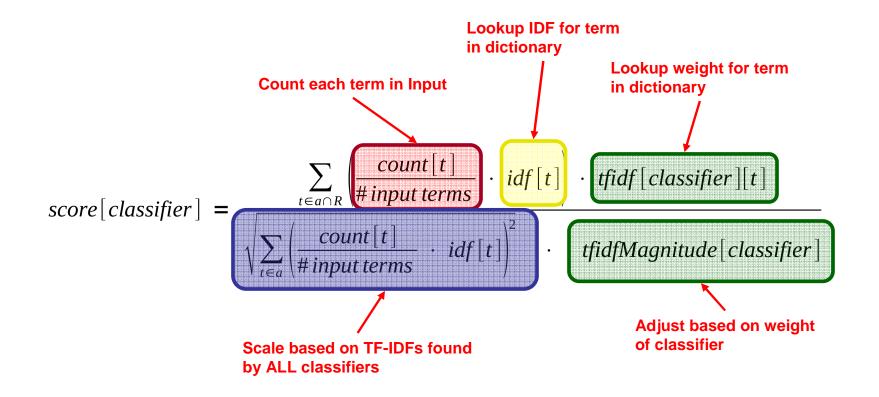






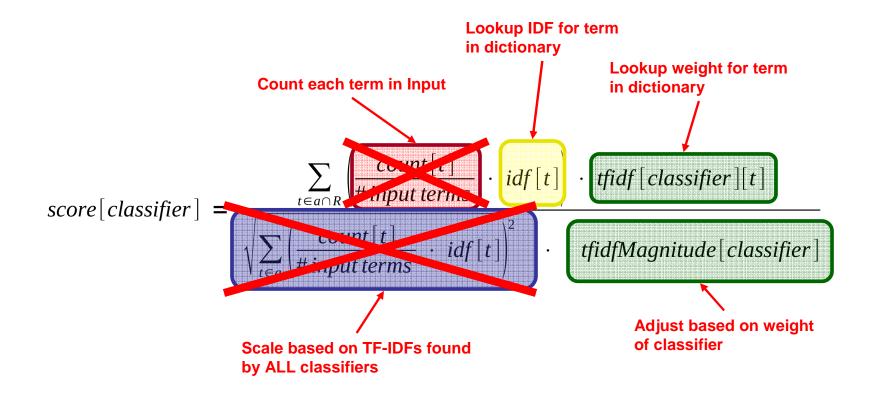








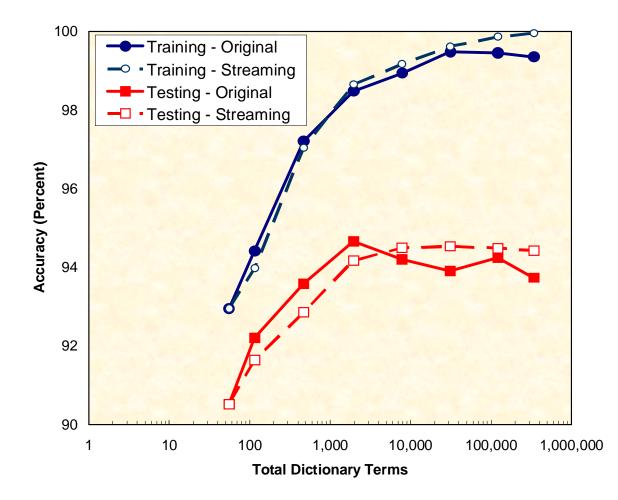








#### **Modification 1: Impact on Accuracy**



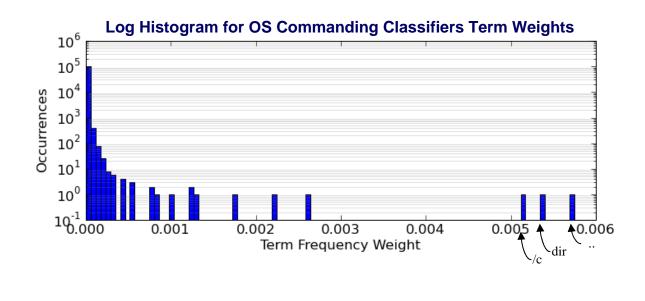






# **Dictionary Observations**

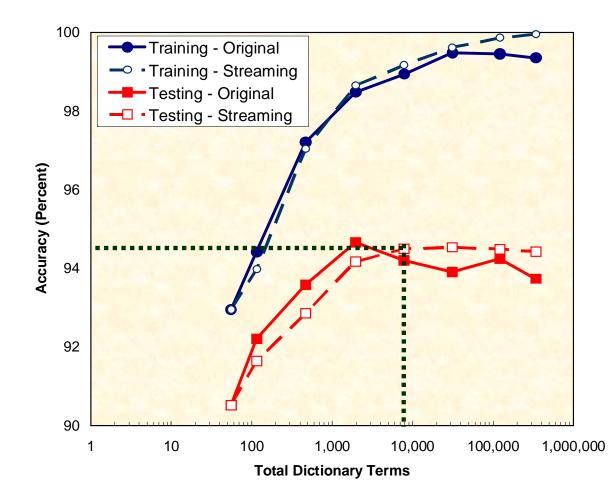
- Many terms in the dictionary
  - 1.8M terms (46MB text, 128MB data)
  - Many terms are junk ("rv:0.7.8"), but they also get very low weight
- Data values are not very diverse
  - Total unique values is < 2% of population</li>
  - Eg: OSC Classifier has 102K terms, but only 415 unique weights







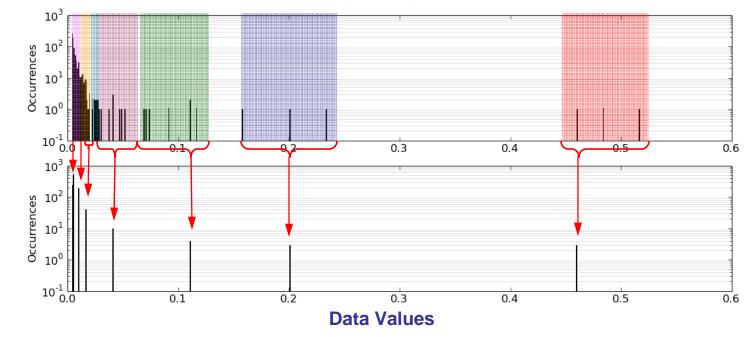
## **Modification 2: Truncate Dictionary**







# **Modification 3: Re-Quantize Data Values**

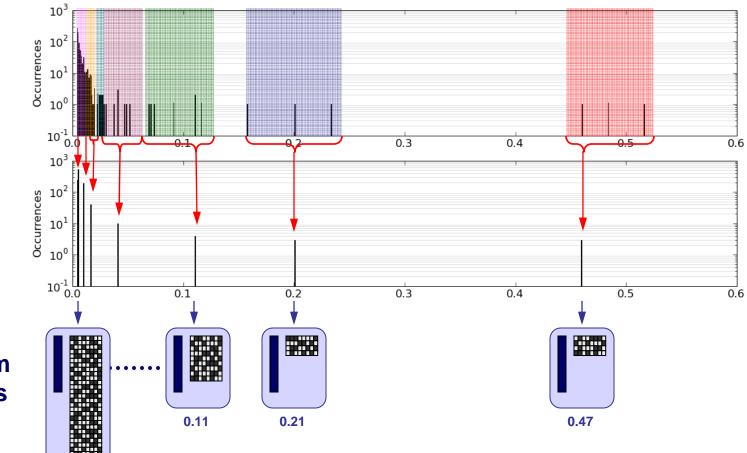


Log-Histogram





#### Modification 4: Map to Q Bloom Filters



Bloom Filters

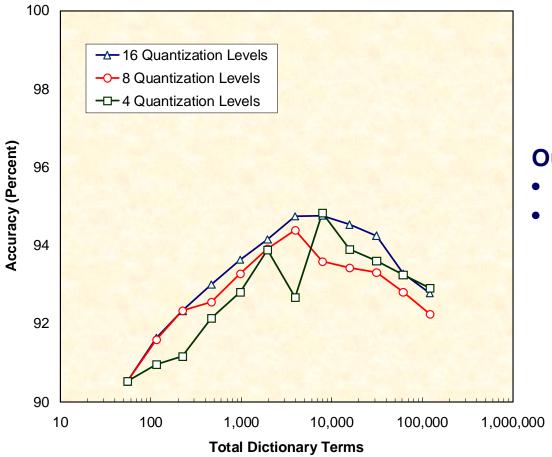








#### **End Impact on Accuracy**



#### **Our Choice:**

- 8 quantization levels/classifier
- 4K total terms







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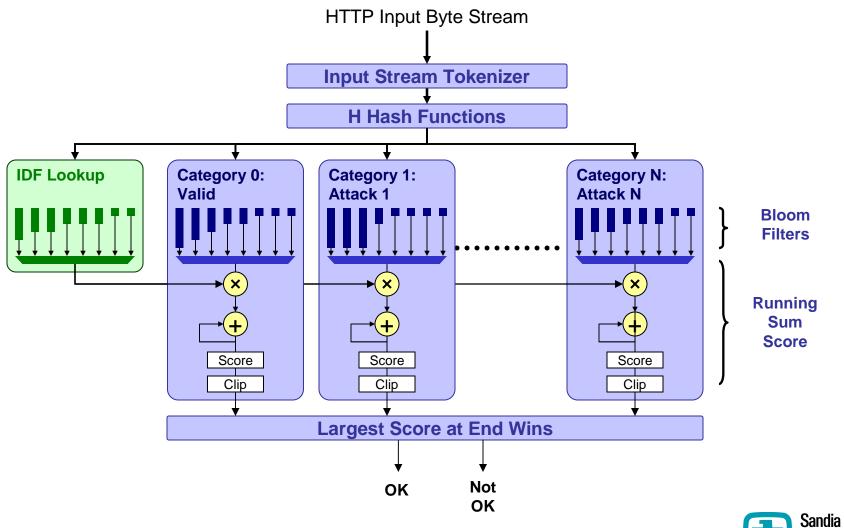
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#### **Core Architecture**



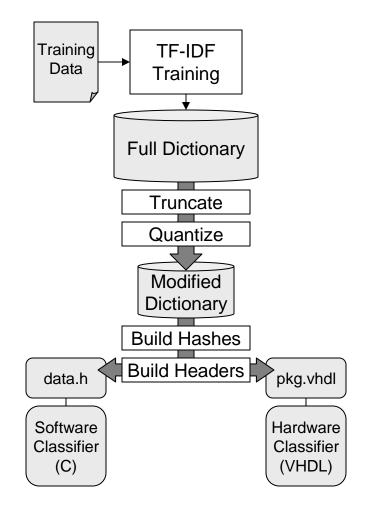






# **Build Flow**

- Desire tools for automatic generation
  - Infrequently rebuild and deploy
  - Utilize in other applications
- User provides
  - Labeled training data
  - Number of dictionary terms
  - Number of hash functions
  - Quantization levels
  - Bloom filter error rate
- Tool chain generates header files
  - C header or VHDL package
  - Static classifier software/hardware
  - Requires a rebuild of design









- Built and tested on Xilinx ML555 board
  - Xilinx Virtex5 LX50T -1 FPGA
  - Target GigE speeds (125MB/s)
  - Maximum clock rate: 196MHz
- Bottleneck: Input tokenizing/hashing
  - Byte stream interface



- Append each token with 2-byte length during hashing
- Results in extra stall cycle between tokens

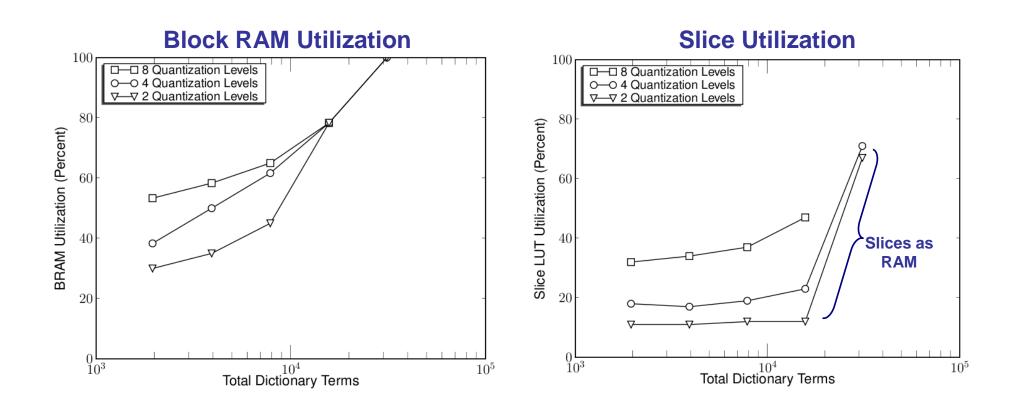
Situation	Efficiency	Rate @ 196MHz
Worst case	0.50	98 MB/s
Best case	0.99	194 MB/s
Average for actual data	0.85	166 MB/s







#### **Resource Utilization**









# **Future Directions**

- Architecture improvements
  - Hybrid hashing: employ efficient hash structure for housing one-offs
  - Transition from compile-time data to run-time data
- Additional platforms
  - Tilera: Assign Bloom filters to different processor cores
  - GPU: Possible, but less attractive due to lack of network options
- Application
  - Apply to other data classification applications
  - Continued work in applying data classification techniques







# **Examining the Algorithm**

- Term-Frequency, Inverse Document Frequency
  - TF: How often does each term appear in an attack?
  - IDF: How specific is the term to an attack?

$$tfidf(t,d) = \underbrace{\frac{count(t,d)}{\sum_{v \in d} count(v,d)}}_{Term \, Frequency} \cdot \underbrace{\log \frac{|D|}{|[d_j:t \in d_j]|}}_{Inverse \, Document \, Frequency}$$

- Cosine Similarity
  - Vector dot product: estimate angle between input and each attack category

$$\operatorname{sim}_{\cos}(a,R) = \frac{\vec{a} \cdot \vec{R}}{\|\vec{a}\| \cdot \|\vec{R}\|} = \frac{\sum_{t \in a \cap R} t f i df(t,a) \cdot t f i df(t,R)}{\sqrt{\sum_{t \in a} t f i df(t,a)^2} \cdot \sqrt{\sum_{t \in R} t f i df(t,R)^2}}$$



